Comparative Analysis of Nano Scaled Low Power 4T SRAM Cell at Various Technology Nodes

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Abstract— In this paper, the study of 4T SRAM Cells which has been one of the versatile circuits in digital circuit design. The variation of parameters like Power dissipation and Total propagation delay with respect to Vdd and Temperature has been analysed in 45nm, 65nm and 90nm technology. TANNER EDA simulation tool has been used for simulation of various parameters of SRAM Cells. In this work, graphs have been drawn for power dissipation and delay in all operations of the cells.

Keywords— VLSI, VDD, SRAM, SPICE, RWM, Delay, Power, Temperature

I. INTRODUCTION

Very Large-Scale Integration is the process of placing thousands (or hundreds of thousands) of electronic components on a single chip. Nearly all modern chips employ VLSI architectures, or ULSI (ultra large scale integration). An SRAM (Static Random Access Memory) is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption [3]. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. Figure 1 shows a typical PC microprocessor memory configuration.

![Figure 1 Typical PC microprocessor memory Configuration](image)

Fast low power SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory. Simultaneously, power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances [5].

4T SRAM Cell

Cell Structure

The 4T SRAM Cell shown in Figure 2, the resistors are replaced with the two PMOS transistors. This cell shows greater stability and low power dissipation as compared to the cell in this section. PMOS being a semiconductor device, consume less power as compared to the resistors used in previous cell.

![Figure 2 4T SRAM cell](image)

The cell size is 35.45% smaller than a conventional 6T cell using same design rules. Read operation performed from one side and write operation performed from other side of cell.
Also swing voltages reduced on word lines during read/write operation. Thus the dynamic energy consumption reduced during read and write operation. Figure 2 shows a circuit equivalent to a developed 4T SRAM cell using supply voltage of 1.1V in 45nm CMOS technology. When ‘0’ stored in cell, load and driver transistor are ON and there is feedback between ST node and STB node, therefore ST node pulled to GND by drive transistor and STB node pulled to VDD by load transistor. And when ‘1’ stored in cell, load and driver transistor are OFF and for data retention without refresh cycle following condition must be satisfied.

\[
I_{off-NMOS-access} \geq 3 \times (I_{DS-Load} - I_{G-Drive}) \quad \text{……………… (1)}
\]

\[
I_{off-PMOS-access} \geq 3 \times (I_{DS-Drive} - I_{G-Load}) \quad \text{……………… (2)}
\]

For satisfying above condition when ‘1’ stored in cell, we use leakage current of access transistor, especially sub threshold current of access transistors. For this purpose during idle mode (when read and write operation don’t performed on cell) of cell, BL and BLB maintained at VDD and GND, respectively and word line1 and word line2 maintained on VIdle1 and VIdle2, respectively. Most of leakage current of access transistors is sub threshold current since these transistors maintained in sub threshold condition. Simulation result in standard 45nm technology shows if during idle mode of cell, BL and BLB maintained at VDD and GND respectively, and VIdle1=0.5V and VIdle2=1.1V ‘1’ stored in cell without refresh cycle and then in idle mode [4].

Write and Read Operation

When a write operation is issued the memory cell will go through the following steps.

1) Bit line driving: For a write, complement of data placed on BLB, and then word line1 asserted to VDD, but voltages on word line2 and BL maintained at idle mode (Vword line2=VIdle2 and VBL=VDD).
2) Cell flipping: This step includes two states as follows. (a) Complement of data is zero: In this state, STB node pulled down to GND by NMOS access transistor, and therefore the drive transistor will be OFF, and ST node will be floated and then pulled up to voltage of BL (VDD) by leakage current (most of this current is sub threshold current) of PMOS access transistor, and thus load transistor will be OFF. (b) Complement of data is one: In this state, STB node pulled up to VDD-Vth by NMOS access transistor, and therefore the drive transistor will be ON, and ST node will be pulled down to GND, thus load transistor will be ON and STB node pulled up to VDD.
3) Idle mode: At the end of write operation, cell will go to idle mode and word line1 and BLB asserted to VIdle1 and GND respectively. When a read operation is issued the memory cell will go through the following steps. (a) Bit line Pre-charging: For a read, BL pre-charged to VDD, and then floated. Since, in idle mode BL maintained at VDD, this step didn’t include any dynamic energy consumption. (b) Word line activation: in this step word line2 asserted to GND and two states can be considered:

- **Voltage of ST node is low**: When, voltage of ST node is low, the voltage of BL pulled down to low voltage by PMOS access transistor. We refer to this voltage of BL as VBL-Low.
- **Voltage of ST node is high**: When voltage of ST node is high, the voltage of BL and ST node equalized (we refer to voltage of BL in this state as VBL-High). Since in this state, there is very small different between BL and ST node, power consumption is very small.

Sensing: After word line2 deactivate the sense amplifier is turned on to read data on BL. Figure 2 shows circuit schematic of sense amplifier that used for reading data from new cell.

Idle mode: At the end of read operation, cell will go to idle mode and word line2 and BL asserted to VIdle2 and VDD, respectively [6].

**Power Consumption of 4T SRAM Cell**

There are four primary capacitances in 4T SRAM cell. These capacitances include BL and BLB capacitances, word lines capacitance, ST capacitance and STB capacitance. BL and BLB capacitances are mainly composed drain junction capacitance of access transistor of 4T SRAM cell. Next large capacitance in 4T SRAM cell is word lines capacitance and mainly composed of gate capacitance of access transistors of 4T SRAM cell. And finally next capacitances in 6T SRAM cell are ST capacitance and STB capacitance. These capacitances mainly composed drain junction capacitance of access transistors of 4T SRAM cell and gate capacitances and drain junction capacitance of PMOS load transistors and NMOS drive transistors [11].

Average power delivered by the circuit initially on the side of the \(V_{in}\) is

\[
P_{av-4T-V_{in}} = \left[ \frac{1}{T} \int_0^T I(t) \, dt \right] \times V_{in} \quad \text{…………………….. (3)}
\]

Here \(P_{av-4T-V_{in}}\) = average power of 4T from \(V_{in}\) supply

\[
P_{av-4T-V_{in}} = 5.483 \times 10^{-6} \text{ w} \quad \text{…………………….. (4)}
\]

Average power on the output of the circuit is

\[
P_{av-4T-V_{out}} = \left[ \frac{1}{T} \int_0^T I(t) \, dt \right] \times V_{out} \quad \text{……………… (5)}
\]

\[
P_{av-4T-V_{out}} = 3.928 \times 10^{-19} \text{ w} \quad \text{……………… (6)}
\]

Power consumed by the 4T memory cell is

\[
P_{\text{consumed-4T}} = P_{av-4T-V_{in}} - P_{av-4T-V_{out}} = 5.482 \times 10^{-6} \text{ w} = 0.5482 \mu\text{w} \quad \text{………………………….. (7)}
\]
II. CIRCUIT DIAGRAM

In this schematic, the 2 PMOS and 2 NMOS transistors are used. The length and width of these are to be set like length is equal to the technology and width is double to the length. In this, the input terminals WL1 is equal to Vdd and WL2 is equal to idle voltage 1.1, BL and BLBAR is complimentary to each other. And the output terminals ST and STB obtained complimentary to each other corresponding to BL and BLBAR. Simulation is done on three technologies 45nm, 65nm and 90nm. And calculate the power dissipation and Delay with the variations of Vdd and Temperature.

III. SIMULATION & RESULTS

Effect of variation of Vdd on Power

<table>
<thead>
<tr>
<th>Technology</th>
<th>45nm</th>
<th>65nm</th>
<th>90nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd(V)</td>
<td>POWER (µW)</td>
<td>POWER (µW)</td>
<td>POWER (µW)</td>
</tr>
<tr>
<td>1.2</td>
<td>0.0028</td>
<td>13.04</td>
<td>17.34</td>
</tr>
<tr>
<td>1.4</td>
<td>0.0045</td>
<td>20.35</td>
<td>27.76</td>
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<td>0.0067</td>
<td>30.8</td>
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<td>1.8</td>
<td>0.0065</td>
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Effect of Variation of Vdd on Delay

<table>
<thead>
<tr>
<th>Technology</th>
<th>45nm</th>
<th>65nm</th>
<th>90nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd(V)</td>
<td>DELAY (ps)</td>
<td>DELAY (ps)</td>
<td>DELAY (ps)</td>
</tr>
<tr>
<td>1.2</td>
<td>29.01</td>
<td>7.85</td>
<td>7.9</td>
</tr>
<tr>
<td>1.4</td>
<td>15.18</td>
<td>6.4</td>
<td>7.66</td>
</tr>
<tr>
<td>1.6</td>
<td>12.2</td>
<td>5.19</td>
<td>4.41</td>
</tr>
<tr>
<td>1.8</td>
<td>8.28</td>
<td>3.85</td>
<td>7.35</td>
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</table>
Effect of Variation of Temperature on Power

Table 3 Power with the variation of Temperature

<table>
<thead>
<tr>
<th>Technology</th>
<th>45nm</th>
<th>65nm</th>
<th>90nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEMP(°C)</td>
<td>POWER (µW)</td>
<td>POWER (µW)</td>
<td>POWER (µW)</td>
</tr>
<tr>
<td>100</td>
<td>0.0084</td>
<td>2.06</td>
<td>3.08</td>
</tr>
<tr>
<td>200</td>
<td>0.0098</td>
<td>6.76</td>
<td>7.75</td>
</tr>
<tr>
<td>300</td>
<td>0.521</td>
<td>1.34</td>
<td>2.4</td>
</tr>
</tbody>
</table>

![Figure 7 Variation of Power with respect to Temperature](image)

Effect of Variation of Temperature on Delay

Table 4 Delay with the variation of Temperature

<table>
<thead>
<tr>
<th>Technology</th>
<th>45nm</th>
<th>65nm</th>
<th>90nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEMP(°C)</td>
<td>DELAY (ps)</td>
<td>DELAY (ps)</td>
<td>DELAY (ps)</td>
</tr>
<tr>
<td>100</td>
<td>3.53</td>
<td>9.312</td>
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<td>200</td>
<td>8.8</td>
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</tr>
<tr>
<td>300</td>
<td>15.9</td>
<td>24.21</td>
<td>15.71</td>
</tr>
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</table>

![Figure 8 Variation of Delay with respect to Temperature](image)

IV CONCLUSION

Simulation of memory cells has been performed in TANNER EDA (14.11v). In simulation work, operations were analyzed through waveforms and output files obtained. Power and Delay are the important factors calculated in this work. First factor is power. Second performance factor is delay. Delay determines speed of memory cell for reading or writing the data. Delay has been obtained by reading the waveforms time duration after which the data becomes stable at a particular voltage level that may be logic ‘0’ or logic ‘1’. In case of 4T SRAM cell, Least Power (0.0016µW) shows at 45nm technology at Vdd 1.2v. Whereas least Delay (1.68ps) shows at 45nm technology at Vdd 1.8v.

REFERENCES


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Variability—A Model-Based Approach” IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 3, MARCH 2011