A Novel Detection and Identification Scheme for Open Switch Faults in PWM-VSI Motor Drive

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Abstract — The objective is to develop a fault diagnose scheme for MOSFET’s open switch faults for PWM voltage source inverter (PWM-VSI) motor drives. Here system monitors line to line voltage as well as switching signals nevertheless the triggering time of MOSFET, under both healthy and faulty conditions. So the measurement of line to line voltage is taken which gives the information about switching states. This can be achieved by a designing simple hardware and can be implemented in the existing motor drive system. The system not only detects the single and multiple faults diagnosis but also minimizes the time taken for fault recognition.

Keywords — MOSFET, line to line voltage, fault recognition, motor drive, PWM voltage source inverter (PWM-VSI)

I. INTRODUCTION

In various industrial applications PWM-VSIs are used for motor drive systems. They are used due to their high switching capability of switching devices. When these drive systems are exposed to the load may lead to the aging which causes damage to motor or drive system, although VSI’s shows better operation but it contain some drawbacks which remain in that condition and operates continuously to improve the consistency, various fault detection strategies are obtained to find open switch faults.

Here [1, 2] the fuzzy logic symptoms are used to find single and multiple-faults and this can be suitable for open and close loop motor drives which permit detection and isolation of faults. Another is [3] the fault detection which is based upon operating characteristics of BLDC motor to maintain control performance under an open-circuit fault and has simple algorithm. Also requires no additional sensors or electrical devices to detect open-circuit faults and this can be embedded into the existing drive software as a subroutine without excessive computation effort. A [4] fuzzy logic used for fault detection and diagnosis in a pulse width modulation voltage source inverter (PWM-VSI) motor drive. The fuzzy technique requires the measurement of the output inverter currents to detect intermittent loss of firing pulses in the inverter power switches. One is dedicated to the healthy domain and the six others to each inverter power switch. This technique is extracted from the current analysis of the fault modes in the PWM-VSI.

Then [5] implementation of real-time condition monitoring algorithm for a three-phase pulse width modulation inverter in a fuzzy controlled induction machine is developed. It is designed to detect and identify the transistor open circuit fault and intermittent misfiring fault, which commonly occurs in the drive system. The condition monitoring mechanism is based on discrete wavelet transform and fuzzy logic.

The [6] fast-diagnostic method is implemented for open-switch faults in inverters without sensors to improve the reliability of power electronic system. This is achieved by analysis of switching function model of the inverter under both healthy and faulty conditions. The open-circuit faults can be detected by sensing the collector–emitter voltages of the lower power switches in each leg. This method minimizes the detection time and is available for the inverter faults in the systems with open-loop or closed-loop current control strategies. This task is performed based on simple hardware and without voltage sensor. This [7] technique is based on the gate-voltage behaviour at turn-On transient of the IGBTs. The detection time is less than 3 µs.

The system shows detection and identification technique for MOSFET’s open-circuit faults in the switching devices of PWMVSI- fed induction motor drives. The measured output quantities used for the FDI scheme are the output line-to-line voltages, but here, such a technique is used that does not compare the output voltages with their respective references, but instead aims at improving the previous effort on two aspects. The first one is that it requires two voltage sensors instead of three. The second is that it permits to reduce diagnosis time to a maximum of one switching period instead of fourth of the fundamental current period. This is done by analysis of the pattern of switching signals and also changes in line-to-line voltage levels under both healthy and faulty operating modes. This can be implemented by addition of simple circuit to existing three phase inverter hardware.

II. PROPOSED HARDWARE

The proposed hardware system is shown in Fig 1. Here the three phase 120° conduction inverter is implemented using IRF540N MOSFET by taking DC voltage as input source. To drive these switching devices we make use of PWM signals which are given to the gate terminal of switching devices. These PWM pulses are generated by Universal VLSI Moon1board which has XC3S400PQ208 FPGA controller and these six PWM signals are given to six MOSFET’s through the interfacing and driving circuit. The FPGA output is given
to buffer IC and given to the opto isolator which prevents the low power circuit from high power circuit and avoids noise.

When the fault is occurred it displays on LED according to the output of AND gate from a generation of fault signals block. Here all LED’s are ON and when the fault occurs the respective LED from all them becomes OFF.

IV. GENERATION OF PWM SIGNALS

The PWM control signals are generated by using Universal VLSI Moon1 board which has XC3S400PQ208 FPGA controller. The program is done in Xilinx ISE 8.1i software and also simulation of six PWM signals is observed. The flow chart for PWM signals is shown in Fig 2 and simulation of PWM control signals is shown in Fig 3.

III. WORKING PRINCIPLE

The system shows detection and identification technique for MOSFET’s open-circuit faults in the switching devices of VSI-fed motor drives. The FDI consists of three blocks: voltage sensing, comparison and voltage detection, generation of fault signals. The measured output quantities used for the FDI scheme are the output line-to-line voltages. Such technique is used that monitors the output line-to-line voltage levels according to the control signals applied on the gates of the switching devices. This line-to-line voltage can be realized by a resistive voltage divider which is output of three phase inverter. The three voltage levels are defined as positive level \(v_{dc}\), zero level \(0\), and negative level \(-v_{dc}\). The FDI detects the zero level change after the fault occurrence from zero level \(0\) to positive level \(v_{dc}\), or from zero level \(0\) to negative level \(-v_{dc}\). However, next will be the comparison and voltage level detection which uses simple circuit based on two voltage comparators and two transistors.

The output of the resistive voltage divider is compared to a negative reference voltage with Comparator-I to detect the fault occurrence in transistor e.g. T1 or T5, and also compared to a positive reference voltage with Comparator-II to detect an open-circuit fault in transistor e.g. T2 or T4. To detect whether the inverter shows an open-circuit fault, a simple logical circuit which generates a fault signal is adopted. In this circuit, the detection of the fault occurrence is achieved by combining the output of each transistor and the reference switching signals applied on the gates of the power semiconductors.
V. RESULTS

Above fig 4 shows the total system which includes FPGA controller board, 3 phase inverter and fault detection and identification circuit. Fig 5 shows the hardware of fault detection and identification circuit which is going to find the open switch damages in switching devices. In fig 6 the PWM control signals are obtained from the Universal VLSI Moon1 board. Also fig 7 shows the line to line voltage obtained from the inverter. So this line to line voltage is further applied to the FDI circuit to find out the open circuit faults of the switching devices.

Now when the drain terminal of Q2 MOSFET is open then the fault is occurred and there is a change in the output line to line voltage than the output of healthy inverter. Fig 8 shows the fault occurred in Q2 MOSFET. The fig 9 shows fault occurred in Q1 MOSFET. When the fault is occurred in switching device the fault detection and identification circuit detects the change in output line to line voltage and on basis of that also with the help of switching signals it identifies which MOSFET if faulty to prevent from degradation of output from the motor drive system and to work efficiently.

VI. CONCLUSION

Here we can detect the open circuit faults of MOSFET for PWM-VSI motor drive and can be obtained by analyzing the line to line voltage levels under both healthy and faulty conditions along with switching signals. When any of the given fault occurs the there is a change in the voltage levels and also in the shape of output waveform. The fault detection and identification circuit senses these changes in the voltage levels and shows the fault in the inverter. With the help of FPGA development board we are able to change PWM frequency without change in program. Also the main advantage of this system that we can detect the fault in running mode we need not have to breakdown the system the find out the open circuit fault.

REFERENCES


